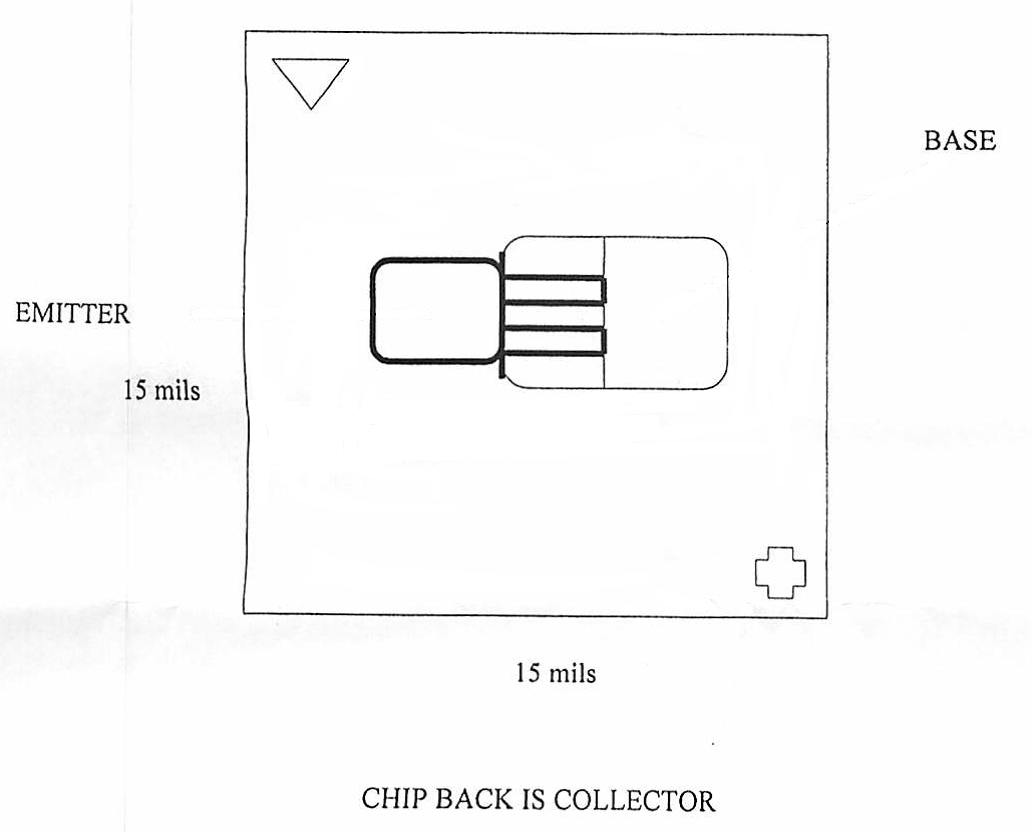
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.015”**

**.015”**



**EMITTER**

**BASE**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: E = .003” X .004” B = .003” X .0045”**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 10/18/21**

**MFG: MOTOROLA THICKNESS .007” P/N: 2N3960**

**DG 10.1.2**

#### Rev B, 7/19/02